PAPER ID-311725

Roll No: 2 2 0 0 5 4 0 1 0 0 1 7 7

BTECH
(SEM III) THEORY EXAMINATION 2023-24
COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 3HRS **M.MARKS: 70**

Note: 1. Attempt all sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief.

Q no.	Question	Marks
a.	What are the different types of Buses used in computer architecture?	2
b.	Name the different types of multipliers.	2
c.	What are the different phases of an instruction cycle?	2
d.	How does control unit of a computer works?	2
e.	Write a short not on locality of reference.	2
f.	Define 2 ½ D memory organization.	2
g.	In what way synchronous and asynchronous serial modes of data transfer differ?	2

SECTION B

2. Attempt any *three* of the following:

a.	What is meant by the term BUS arbitration? Why is it needed? How can bus arbitration be implemented in Daisy changing scheme?	7
b.	Show the multiplication process using Booth's algorithm when the following numbers are multiplied: - (-12) *(-18).	7
c.	What is pipelining? What are the different stages of pipelining? Explain in detail.	7
d.	Give classification of memory based on the method of access. Also discuss construction and working of magnetic disk and various components of disk access time.	7
e.	What are the basic differences between interrupt initiated I/O and programmed I/O? Explain in detail.	7

SECTION C

3. Attempt any *one* part of the following:

a.	What do you mean by processor organization? Explain various types of processor organization with suitable example.	7
b.	Differentiate between Memory stack and register stack.	7

4. Attempt any *one* part of the following:

a.	Explain in detail the principle of carry looks ahead adder and design 4-bit CLA adder.	7
b.	Represent the following decimal number in IEEE standard floating-point format in a single precision method (32 bit) representation method. (i) $(85.125)_{10}$ (ii) $(-307.1875)_{10}$	7

5. Attempt any *one* part of the following:

a.	Explain the different cycles of an instruction execution.	7
b.	Differentiate between hardwired and micro programmed control unit. Explain each component of hardwired control unit organization.	7

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6. Attempt any *one* part of the following:

a.	Consider a cache (M1) and memory (M2) hierarchy with following characteristics: - M1 : 16K word, 50 ns Access time M2 : 1M word, 400 ns Access time Assume 8-word cache blocks and set size 256 words with set associative mapping. (i) Show and explain the mapping between M2 and M1. (ii) Calculate the effective memory access time with cache hit ratio=0.95.	7
b.	Explain the direct mapping technique. Consider a digital computer has a memory unit of 64k*16 and cache memory of 1k words. The cache uses direct mapping with 4 block size of four words. (i) How many bits are there in the tag, block and word fields of the address format? (ii) How many blocks can the cache accommodate?	7

7. Attempt any *one* part of the following: **7 x 1 = 7**

a.	What do you mean by asynchronous data transfer? Explain strobe control and handshaking mechanism.	7
b.	Explain the various modes of data transfer and discuss direct memory access mode in detail. Also explain how DMA is superior to other modes.	7

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