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**Printed Pages: 2** **Sub Code: NMCA 215**

**Paper Id:** | 2 | 1 | 4 | 2 | 1 | 4 | **Roll No.** | | | | | | | | | | |

**MCA**
**(SEM II) THEORY EXAMINATION 2017-18**
**COMPUTER ORGANIZATION**

***Time: 3 Hours*** ***Total Marks: 100***

**Note:** Attempt all Sections. If require any missing data; then choose suitably.

**SECTION A**

**1. Attempt *all* questions in brief. 2 x 10 = 20**

a. Show the block diagram of hardware that implement the following register transfer statement :

yT2 : R2 ← R1, R1 ← R2

b. Define selective-set micro-operation.
c. How arithmetic operations are performed?
d. What do you mean by program counter?
e. A computer has 32 bit instructions and 8 bit address. If there are 250 three address instructions, how many two address instructions can be formulated?
f. Given the 16 bit value 1001101011001101. What operations must be performed in order to : clear to 0 the first eight bits and complement the middle eight bits?
g. What do you mean by I/O bus?
h. Define external interrupts.
i. What do you mean by address map?
j. Define hit ratio.

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**SECTION B**

**2. Attempt any *three* of the following: 10 x 3 = 30**

a. A digital computer has a common bus system for 16 registers of 32 bit each. The bus is constructed with multiplexers.
   (i) How many selection inputs are there in each multiplexer?
   (ii) What sizes of multiplexers are needed?
   (iii) How many multiplexers are there in a bus?
b. Write short note on hardwired control unit.
c. Discuss RISC and compare RISC with CISC.
d. Explain serial communication in detail.
e. Extend the memory system of 128X8 RAM chips and 512X8 ROM chips to 4096 bytes of RAM and 4096 bytes of ROM. List the memory address map and indicate what size of decoders are needed.

**SECTION C**

**3. Attempt any *one* part of the following: 10 x 1 = 10**

(a) Starting from an initial value of R=11011101, determine the sequence of binary values in R after a logical shift left, followed by a circular shift right, followed by a logical shift right and a circular shift left.
(b) Show the step by step multiplication process using Booth algorithm for (+15) X (+13).

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**4. Attempt any *one* part of the following: 10 x 1 = 10**

(a) Explain wide-branch addressing and micro-program sequencing.

(b) Discuss instruction with next-address field with neat diagram.

**5. Attempt any *one* part of the following: 10 x 1 = 10**

(a) A first-in, first-out (FIFO) has a memory organization that stores information in such a manner that the item that is stored first is the first item that is retrieved. Show how a FIFO memory operates with three counters. A write counter WC holds the address for writing into memory. A read counter RC holds the address for reading from memory. An available storage counter ASC indicates the number of words stored in FIFO. ASC is incremented for every word store and decremented for every item that is retrieved.

(b) The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields : an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word.

**6. Attempt any *one* part of the following: 10 x 1 = 10**

(a) Explain interrupt handling routine with the help of flow charts.

(b) Describe CPU-IOP channel communication in the IBM370 in detail.

**7. Attempt any *one* part of the following: 10 x 1 = 10**

(a) Explain FIFO, LRU and OPT page replacement algorithms with example.

(b) Explain various cache memory mapping techniques.

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