Printed pages: 01 **Sub Code: VL922**

Paper Id: 208216 **Roll No:** | | | | | | | | | | |

M TECH

(SEM-II) THEORY EXAMINATION 2017-18

SOC DESIGN

Time: 3 Hours ***Total Marks: 100***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

I. Attempt *all* questions in brief. **2 x 10 = 20**

a. Distinguish between energy and power dissipation of VLSI circuits.
b. Draw SoC Design flow.
c. What are the applications of system level design of Soc devices?
d. What do you mean by Network on Chip?
e. What is Cache coherence?
f. What are four generations of Integration Circuits? Also write the capacity of each generation.
g. What are the typical goals in SoC design?
h. What are the advantages of CMOS process?
i. Write down about Interconnect for SoC.
j. What do you mean by Low Power VLSI?

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

a. Write a note on Specification requirement in SOC design.
b. With the neat flow chart explain the high level verification for an SOC device.
c. What is the different power management circuit in Soc.? What are the different sources of power dissipation?
d. What do you mean by system level design of Soc devices? Also explain the various system level design issues.
e. Describe different switching techniques used in NOC.

SECTION C

3. Attempt any *one* part of the following: **10 x 1 = 10**

a. What do you mean by Packet switching and wormhole routing? Explain.
b. Write a note on the analysis of Performance for MPSoCs design.

4. Attempt any *one* part of the following: **10 x 1 = 10**

a. Explain about the top down vs. bottom up approach of SoC desigu.
b. Explain about a canonical SoC Design.

5. Attempt any *one* part of the following: **10 x 1 = 10**

a. Write short note on techniques for designing MPSoCs.
b. Discuss the tools and techniques used for designing. verifying and implementing SOC using programmable logic.

6. Attempt any *one* part of the following: **10 x 1 = 10**

a. Explain about the hardware Aecclerators in SoC.
b. What do you mean by Design for timing closure?

7. Attempt any *one* part of the following: **10 x 1 = 10**

a. Write down about the techniques for designing MPSoCs.
b. Write a note on low power open multimedia application for 3G wireless communication technology.