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Following Paper ID and Roll No. to be filled in your Answer Book.

PAPER ID : 33218 Roll No.

B. Tech. Examination 2023-24

(Even Semester)

COMPUTER ORGANIZATION & ARCHITECTURE

Time : Three Hours] *[Maximum Marks : 60*

Note :– Attempt all questions.

SECTION – A

1. Attempt all parts of the following : 8×1=8

   (a) What is cache memories?

   (b) What do you mean by register?

   (c) What is synchronous communication?

   (d) What is semiconductor RAM memories?

   (e) Explain two difference between horizontal and vertical microprogramming.

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(f) What is auxiliary memories?

(g) What is prefetching?

(h) Define the term computer architecture.

SECTION – B

2. Attempt any two parts of the following : 2×6=12

(a) Explain the different bus architecture and its types with block diagram.

(b) Show the systematic multiplication process when (+20) × (–19) are multiplied, using Booth's algorithm.

(c) Write short notes on the following :

(i) Address mapping

(ii) Magnetic disk

(iii) ROM memories

(d) Explain in detail about the different types of interrupts and exceptions.

SECTION – C

Note :– Attempt all questions. Attempt any two parts from each questions. 8×5=40

3. (a) Explain Von Neumann architecture in detail (with necessary diagram).

   (b) What are the different bus arbitration techniques? Explain in detail.

   (c) What are the advantages and disadvantages of multiple bus organization over a single bus organization?

4. (a) What is pipelining? What are the major characteristics of a pipeline?

   (b) Explain the process of fetching a word from memory and storing a word in memory, with diagram.

   (c) What are different types of addressing modes? Explain in detail.

5. (a) What are the standard communication interfaces?

   (b) Discuss the design of a typical input-output organization processor design.

   (c) Explain I/O channels and processors in detail.

6. (a) What is 2D and 21/2D memory organization?

(b) Explain the basic concept and hierarchy of memory organization.

(c) What are the different mapping techniques used in cache memories?

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