S.No. : 34 BCS 2404

No. of Printed Pages : 05

Following Paper ID and Roll No. to be filled in your Answer Book.

PAPER ID : 23210 Roll No.

B. Tech. Examination 2017-2018

(Fourth Semester)

COMPUTER SCIENCE AND ENGINEERING

(Computer Organization and Architecture)

Time : Three Hours] *[Maximum Marks : 60*

Note :– Attempt all questions.

SECTION–A

1. Attempt all parts of the following : $8 \times 1 = 8$

   (a) Define computer organization.

   (b) What do you mean by locality of reference.

   (c) What is instruction register (IR) and program counter (PC) wed for?

   (d) Define multitasking.

   (e) What do you mean by assembler directives?

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(f) Define carry save addition process.

(g) What is the role of cache memory in pipeline?

(h) Define Hit and Miss?

SECTION – B

2. Attempt any two parts of the following : $2 \times 6 = 12$

(a) Discuss Van Neumann architecture in detail. Why this architecture is so popular?

(b) A computer has 16 registers an ALU with 32 operations and a shifter with eight operations all connected to common bus system.

(i) Formulate a control word for a microoperation.

(ii) Specify the number of bits in each field of the control word and give a general encoding scheme.

(iii) Show the bits of the control word that specify the microperation $R4 \rightarrow R5 + R6$

(c) Convert the following arithmetic expressions from reverse polish notation to infix notation.

(i) ABCDE + * - /

(ii) ABC */D - EF/+

(d) Why are use hierarchical memory structure? What are the parameters that affects the design of memory hierarchy.

SECTION – C

Note :- Attempt all questions. Attempt any two parts from each question. $8 \times 5 = 40$

3. (a) What is meant by the term bus arbitration? Why is it needed? How can bus arbitration be implemented in daisy chaining?

(b) (i) Discuss the shift micro-operation and its hardware implementation.

(ii) Differentiate between hardware control and microprogrammed control.

(c) Show the hardware that implments the following statement. Include the logic gates for the control function and a block diagram for the binary counter with a count enable input.

$$xyI_3 + T_1 + y'T_2 : AR \leftarrow AR + 1$$

4 (a) Explain linear pipelines. Differentiate between asynchronous and synchronous models of linear pipelines.

(b) (i) Discuss micro instruction with next address field.

(ii) What is an op code? How many bits are needed to specify 3z distinct operations and why?

(c) What is the difference between a direct and an indirect address instruction? How many references to memeory are needed for each type of instruction to bring an operand into a processor register?

5. (a) Explain any three addressing modes in detail by giving examples.

(b) Discuss in detail with diagram the concept of Direct Memory Access.

(c) What are the reasons for having interrupts in computer? How can the interupt be handled in computer? Suggest a scheme that can handle multiple interrupts at a time.

6. (a) An 8- bit compufer has a 16-bit address bus. The first 15 lines of the address are used to select a bank of 32k bytes of memory. The high order bit of the address is used so select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32k bytes each for a total of 256K bytes of memory.

(b) A digital computer has a memory unit of 64K x 16 and a cache memory of 1k words. The cache uses direct mapping with a block size of four words.

(i) How many bits are there in the tag, index, block and word fields of the address format?

(ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.

(iii) How many blocks can the cache accomodate?

(c) Discuss statis and dynamic RAM. Explain 2D and $2Y_2D$ (RAM) organization with their merits and demerits.

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