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Following Paper ID and Roll No. to be filled in your Answer Book.

PAPER ID : 23210 Roll No.

B. Tech. Examination 2018-2019

(Even Semester)

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : Three Hours] *[Maximum Marks :60*

Note :– Attempt all questions.

SECTION–A

1. Attempt all parts of the following : $8 \times 1 = 8$

   (a) Write functions of Computer System.

   (b) Define role of Program Counter (PC) in a program execution.

   (c) What is micro instruction and micro operation?

   (d) Define in short what is Pipeline Processing?

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(e) Write Reverse Polish Notation for A* B + A * (B * D + C* E) expression

(f) What is difference between RISC and CISC computers?

(g) What is the function of Read/Write Signal in Memory?

(h) What is Virtual Memory?

SECTION – B

2. Attempt any two parts of the following : $6 \times 2 = 12$

(a) Write the algorithmic steps for BOOTH MULTIPLICATION ALGORITHM with logic circuit and flow chart and apply for the following : (-20) × (+20).

(b) A digital computer system has the following configurations :

(i) Memory : 2096 × 24

(ii) Can perform 2048 operations only

(iii) Indirect Addressing dependent on single I - bit.

(iv) Control Unit implementation dependent on micro programmed control unit architecture. Control unit contains a control memory capable for 1K × 32 words.

Find the following :

(i) Total number of bits required for OPCODE and OPERAND.

(ii) Length of Program Counter (PC), Address Register (AR), Data Register (DR).

(iii) Total number of micro-instruction can be stored in control memory. Length of micro - instruction, Control Address Register (CAR) Subroutine Buffer Register (SBR).

(c) Describe the principle of designing Instruction Set of a program. Explain important field of instruction format. Assume that memory locations A, B, C, D, E, F, G and X should not be changed. Write a program for simple three address, two address, one address and zero address machine to perform.

X = (A + B - C) / (D * (5 * F - G))

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(d) What is the mapping for cache organization? Explain the following with example :

(i) Associative Mapping

(ii) Direct Mapping

(iii) Set Associative Mapping

Consider a cache consisting of 256 blocks of 16 words each, for a total of 4096 (4K) words, and assume that the main memory is addressable by a 16-bit address and it consists of 4K blocks. How many bits are there in each of TAG, BLOCK/SET and word fields for all mapping technique.

SECTION – C

Note:- Attempt any two parts from each questions. $10 \times 4 = 40$

3. Attempt any two parts of the following :

(a) What is REGISTER TRANSFER LANGUAGE? Explain all type of SHIFT OPERATION. The 8-bit registers AR, BR, Cr and DR initially have the following values AR =11110010, BR = 11111111, CR = 10111001, DR = 11101010. Determine the 8-bid values in each register after the execution of the following :

(i) AR ← AR + BR

(ii) CR ← ashr (CR), DR Ishl (AR)

(iii) AR ← AR - CR

(b) Discuss the Direct Memory Acess (DMA) data transfer with the help of block diagram.

(c) What do you understand by Memory Hierarchy? Explain the following property in detail :

(i) Inclusion Property

(ii) Locality of Reference

(iii) Coherence Property

4. Attempt any two parts of the following :

(a) What is an Arithmetic and Logic Operation (ALU)? Draw logic diagram of ALU that performs AND, OR logic operation and ADD, SUB arithmetic operations.

(b) Convert the following symbolic micro operation to register transfer statement :

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(i) READ, INCPC

(ii) ACTDR, DRTAC

(iii) ARTPC, DRTAC, WRITE

Suppose the MICROPROGRAM for ADD routine as follows :

ADD :	READ	I	CALI	INDR 2
	ADD	U	JMP	FETCH

What should be the subroutine for INDR 2.

(c) Draw and explain the architecture of register organization in a computer system. Write the procedure for PUSH and POP operation in the following :

(i) Register Stack

(ii) Memory Stack

5. Attempt any two parts of the following :

(a) Write the algorithmic steps for SIGNED NUMBER DIVISION ALGORITHM with logic circuit and flow chart and apply for the following : (+7) ÷ (+3).

(b) What is Bus Organization in a computer system? Explain the important features of following techniques.

(i) Daisy Chaining Technique

(ii) Polling Technique

(iii) Independent Request Technique

(c) Explain the hit ratio and miss ratio of memory organization. Consider a Cache (M_1), Main Memory (M_2) and Disk Storage (M_3) with following characteristic.

(i) M_1 : 16K word, 50ns access time, c_1 = $ 1.25.

(ii) M_2 : 1M word, 400 ns access time, c_2 = $ 0.2.

(iii) M_3 : 256 M word, 4ms access time, c_3 = ?

The total cost of memory organization is upper bounded by $ 15000. Find cost per word for memory level M_3 and Effective Access Time. Cache hit is given as 0.98; Main hit is given as 0.9.

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6. Attempt any two parts of the following :

(a) What is Instruction Cycle for a program execution? Write the micro-operation for the following cycles :

(i) Fetch Cycle

(ii) Indirect Cycle

(iii) Interrupt Cycle

(b) Defined the addressing mode of an instruction. Explain the following with example : Register, Register Indirect, Direct, Immediate, Implicit, Relative, Indexed, Base Register addressing modes.

(c) A Computer system employs RAM organization of 512 bytes and ROM organization of 512 bytes with the help of 128 x 8 bit RAM chip and 256 x 8 bit ROM chip. Processor has 16 address lines. Find the following :

(i) How many RAM and ROM chip required

(ii) Draw the circuit diagram for interfacing of RAM chips, ROM chips and processor.

(iii) Draw the memory address map.

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