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Following Paper ID and Roll No. to be filled in your Answer Book.

PAPER ID : 33218 Roll No.

B. Tech. Examination 2022-23

(Even Semester)

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : Three Hours] *[Maximum Marks : 60*

Note :– Attempt all questions.

SECTION–A

1. Attempt all parts of the following : 8×1=8

   (a) Differentiate interrrupts and exceptions.

   (b) Define the role of MIMD in computer architecture.

   (c) List three types of control signals.

   (d) Differentiate between RAM and ROM.

   (e) Explain significance of DMA.

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(f) Explain the difference between COM and EXE programmes.

(g) How many bits are there in the data and address input of the memory?

(h) How many 128×8 memory chips are needed to provide a memory capacity 4096×16?

SECTION – B

2. Attempt any two parts of the following : 2×6=12

(a) Perform the division process of 00001111 by 0011 (use a dividend of 8 bits).

(b) Define interrupts. Point out and explain the various ways of enabling and disabling interrupts.

(c) What is mapping? Explain set associative cache mapping techniques.

(d) Explain any five addressing modes with examples.

SECTION – C

Note :– Attempt all questions. Attempt any two parts from each question. 5×8=40

3. (a) Explain the term RAID. What are the techniques used by RAID for enhancing reliability?

(b) Discuss and differentiate between tightly coupled multiprocessor and loosely coupled multiprocessors from the point view of hardware organisation and programming techniques.

(c) How many switch points are there in a Grossbar switch network that connects 'p' processors to 'm' memory modules.

4. (a) Draw the flow chart of Booth's algorithm for multiplication and show the multiplication process using Booth's algorithm for $(-7) \times (+3)$.

(b) What do you understand by Amdahl's law, explain with suitable example.

(c) Register A holds 8 bit binary 1111111. Determine the B operand and the logic micro operation to be performed in order to change the value in A to :

(i) 01101111

(ii) 11111100

5. (a) Consider a computer having 256 word RAM and cache 16 block (block size = 4 words). Where is a memory word location 120 mapped, in cache if :

   (i) Direct mapping is used?

   (ii) 2-way set associative mapping is used?

   (b) Explain various cache write policies.

   (c) Explain the DMA technique for I/O operation.

6. (a) Explain internal organisation of 2M×8 asynchronous DRAM chip.

   (b) Discuss a single-train sistor dynamic memory cell.

   (c) What are the action required to complete instruction ADD (R3), R1.

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