No. of Printed Pages : 05 **BCS 301**

Following Paper ID and Roll No. to be filled in your Answer Book.

PAPER ID : 3203 Roll No.

B. Tech. Examination 2016-2017

(Third Semester)

DIGITAL LOGIC DESIGN

Time : 3 Hours] *[Maximum Marks : 100*

Note :– Attempt all questions. Each question carry equal marks.

1. Answer any four parts of the following : 5×4=20

   (a) Implement NOR gate using NAND gates only.

   (b) Represent the following number in single precision format :

      (i) 0.5

      (ii) –1

   (c) Explain the floating-point data representation for decimal number and binary number. What are the advantages and disadvantages of having different values for bases and radix in floating point number format?

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(d) Using Tabular method and algebraic solution of P. I. table, obtain minimal relization of a function shown below :

$F(A, B, C, D) = \sum (1, 2, 3, 9, 12, 13, 14) + \sum d (0, 7, 10)$

(e) Generate the CRC code for the data word of 110010101. The divisor is 10101.

(f) A seven bit hamming code is received as 1110101. What is the correct code?

2. Answer any two parts of the following : 10×2=20

(a) (i) What is similar between a half adder and a half subtractor?

(ii) Implement a full subtractor circuit using only NAND gates.

(b) (i) Explain how demultiplexer can be used as a decoder?

(ii) With a neat diagram explain the function of an encoder.

(c) (i) Design a odd parity generator for a 3 bit message code.

(ii) Using four-input multiplexers, implement the following function :

$F(A, B, C) = \sum m (0, 2, 3, 5, 7)$

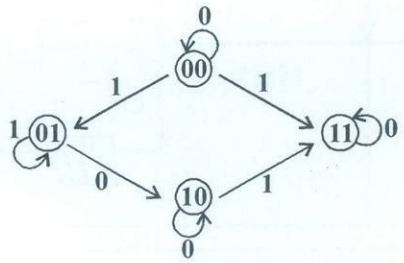
3. Answer any two parts of the following : 10×2=20

(a) (i) What is the basic difference between pulse-triggered and edge-triggered flip-flops?

(ii) If $\bar{Q}$ output of a D-type flip-flop is connected to D input, it acts as a toggle switch. State whether True or False with justification?

(b) By using suitable FFs design a counter to go through the states 0 – 1 – 3 – 4 – 6 – 0. Draw the logic diagram. Examine the action of counter for the unused states.

(c) For the state diagram shown in figure, obtain the state table and design the circuit using minimum number of J-K flip-flop :



4. Answer any two parts of the following : 10×2=20

(a) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transfered to Z. When Y is 0, the output does not change for any change in X. Use SR latch for implementation of the circuit.

(b) (i) Discuss different modes of asynchronous sequential circuits.

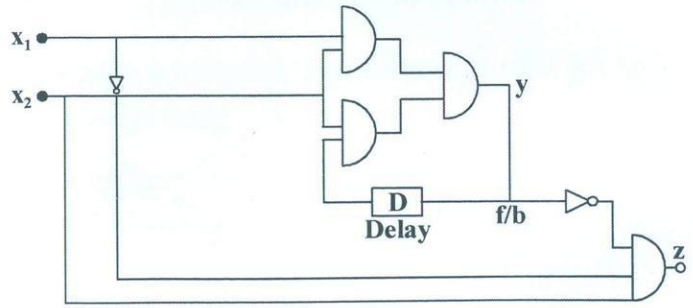
(ii) What are critical and non-critical race? Is race-around condition an example of race? Justify.

(c) Analyze the given circuit, assuming it operate in fundamental mode, using :

(i) Flow table

(ii) Transition flow diagram

(iii) Transition flow table if exists



5. Answer any two parts of the following : 10×2=20

(a) Write short notes on :

(i) PLA

(ii) PAL

(iii) CPLD

(iv) FPGA

(b) (i) Realize the given function using PLA :

$f_1 (A, B, C) = \Sigma (0, 2, 4, 5)$

(ii) Compare Mealy and Moore design of finite state machines.

(c) Using VHDL design :

(i) Traffic lights controller

(ii) Washing machine

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