(b) Given a universal shift register speech its diagram only for left shift operation and explain its working.

(c) Explain the operation of SR laten with circuit diagram, function table and lining diagram.

6. (a) Explain the operation of 3 bit asynchronous up counter.

(b) Write short notes on any one of the following :

(i) CPLD

(ii) PLA

(c) Design PAL for a combinational circuit that squares a 2 bit numbers.

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No. of Printed Pages : 04

Following Paper ID and Roll No. to be filled in your Answer Book.

PAPER ID : 33213 Roll No.

B. Tech. Examination 2021-22

(Odd Semester)

DIGITAL LOGIC DESIGN

Time : Three Hours] *[Maximum Marks : 60*

Note :– Attempt all questions.

SECTION–A

1. Attempt all parts of the following : 8×1=8

(a) Differentiate between analog and digital signal.

(b) Find the excess-3 and gray code of BCD number (0101).

(c) Write the characteristic table of J-K flip-flop.

(d) Distinguish between combinational and sequential circuits.

(e) Realize OR circuit using NOR gates.

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(f) Simplify the following function :

$$F(A, B, C, D) = \overline{(\bar{A}+C)\ (B+\bar{D})}$$

(g) Explain the meaning of FANOUT.

(h) What is the difference between PAL and PLA?

SECTION – B

2. Attempt any two parts of the following : 2×6=12

(a) Explain the Karnaugh map method and simplify the following Boolean expression using K-map :

$$F(A, B, C, D, E) = \Sigma m(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 30, 31)$$

(b) Draw and explain the function of 2 : 1 multiplexer. Write applications of multiplexer.

(c) Explain the difference between latch and flip-flop. Draw and explain the operation of D flip-flop.

(d) Implement the circuit of a PLA with 3 input, 2 output and 4 product terms :

$$F(A, B, C) = \Sigma(3, 5, 6, 7)$$

SECTION – C

Note :– Attempt all questions. Attempt any two parts from each question. 8×5=40

3. (a) Explain cyclic code with example. Convert decimal number 3452 to BCD Code.

(b) Define the terms logic gate and universal logic gate. Explain various basic gates with their symbols and truth table.

(c) Design the circuit using NAND gates for following functions :

$$F = A\,B\,C' + D\,E + A\,B'\,D'$$

4. (a) What is a decoder? Draw and explain 3 : 8 decoder.

(b) Explain half adder circuit and implement full adder circuit using two half adder.

(c) Explain the difference between encoder and multiplexer.

5. (a) Draw and explain the operation of ring counter.